

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:	)	Customer Number: 53080
	)	
U.S. Patent No. 6,455,348	)	Confirmation Number: 2437
	)	
Serial No.: 10/761,098	)	Group Art Unit: 2812
	)	
Filed: January 21, 2004	)	Examiner: Leonard CHANG
	)	
Inventor: Yukio YAMAGUCHI	)	
	)	
For: LEAD FRAME, RESIN-MOLDED SEMICONDUCTOR DEVICE, AND METHOD		
FOR MANUFACTURING THE SAME		

**SUPPLEMENTAL DECLARATION PURSUANT TO 37 C.F.R. § 1.175(b)**

Hon. Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

Sir:

I declare:

**THE INVENTORS**

1. That I, Yukio Yamaguchi, reside at the address listed below, which is also my mailing address, and declare that I am a citizen of Japan; that I was employed by Matsushita Electric Industrial Co., Ltd. of Osaka Japan (now known as Panasonic Corporation as the result of a corporate name change) at the time the above-identified application was filed; that Panasonic is the Assignee of the entire interest of the above-identified patent; that at the time the application for the above-identified Patent was filed I was engaged in the design of lead frames and resin-molded semiconductor devices as described in United States Letters Patent No. 6,455,348

("original patent"), that I do not know and do not believe that the invention was ever known or used in the United States before my invention; and that I am the declarant, applicant and patentee, referred to hereinafter.

2. That I believe I am the original, first and sole inventor of the subject matter of the invention, which is claimed and for which a reissue patent is sought in the above-identified reissue application.

3. That I believe the original patent to be wholly or partly inoperative or invalid, by reason of my claiming less than I had a right to claim. Specifically, new claims 16-25 are directed to a novel resin-molded semiconductor device, which includes, among other elements, a semiconductor chip having electrode pads, a die pad for supporting the semiconductor chip, and inner leads each including a groove so as to define a reduced thickness portion. In a structure including such grooves, even if the lower surface of the signal-connecting leads is not covered with the resin encapsulant, the resin encapsulant can still hold the signal-connecting leads in a sufficiently strong/secure manner. However, the original claims of USP No. 6,455,348 were only directed to a method of manufacturing the resin-molded semiconductor device, and therefore did not recite a resin-molded semiconductor device having inner leads each including a groove. Thus, it was an error not to include a claim directed to a resin-molded semiconductor device having inner leads each including a groove, as I claimed less than I had a right to claim. Further, it is noted that while USP No. 6,081,029 contained claims directed to a resin-molded semiconductor device, these claims did not recite inner leads each including a groove so as to define a reduced thickness portion. As such, the original patents failed to include claims directed to the novel resin-molded semiconductor device having inner leads each including a groove, and

therefore I claimed less than I had a right to claim.

4. That I believe that the error regarding my narrow claiming of the invention arose inadvertently and without deceptive intent.

5. Every error in the patent which is corrected by this reissue application, and is not covered by a prior oath/declaration submitted in this application, arose without any deceptive intent.

6. In accordance with 35 U.S.C. § 120, I claim the benefit of the filing date of prior US application Serial No. 09/244,074 (the '074 application), filed on February 4, 1999, which is now USP No. 6,081,029, and in accordance with 35 U.S.C. § 119, I claim the benefit of a foreign filing date on the basis of Japanese Patent Application No. 10-060811, filed in Japan on March 12, 1998. A certified copy of Japanese priority document was filed in the '074 application that issued as U.S. Patent No. 6,081,029.

7. That I hereby state that I have reviewed and understand the contents of the above-identified reissue application, including the addition of newly added claims 16-25 directed to a resin-molded semiconductor device, which were added by an amendment filed on October 9, 2007.

8. That I acknowledge the duty to disclose information of which I am aware which is material to the patentability of the application for the above-identified reissue application in accordance with 37 C.F.R. § 1.56(a).

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and like so made are

punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: Nov. 19, 2009

Yukio Yamaguchi: Yukio Yamaguchi

Address:

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Shiga-ken 520-2279, JAPAN

WDC99 1791698-1.060188.0747

Docket No.: 060188-0747

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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Yukio YAMAGUCHI	:	Confirmation Number: 2437
Application No.: 10/761,098	:	Group Art Unit: 2812
Filed: January 21, 2004	:	Examiner: Leonard CHANG
For: LEAD FRAME, RESIN-MOLDED SEMICONDUCTOR DEVICE, AND METHOD FOR MANUFACTURING THE SAME		

**ASSENT OF ASSIGNEE TO REISSUE**

Mail Stop REISSUE  
Hon. Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

Sir:

The undersigned, by authority vested in him by Panasonic Corporation (formerly Matsushita Electric Industrial, Co., Ltd.), assignee of the entire interest in the above-identified Letters Patent, the invention described therein, and in any reissue thereof by assignment recorded at Reel 9753, Frame 0250, hereby assents on behalf of the assignee to the accompanying reissue application.

I hereby declare that I have been empowered with the authority to consent to the above-

identified reissue application and sign this document on behalf of Panasonic Corporation.

Date: Nov. 13, 2007

Director, IP Development Center  
Title: Authorized Signing Officer

Name: Hiroki Naito

Signature: 